AF/GA ~~2811~~

PATENT
Attorney Docket No. 2915.1US (96-149.01)

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Devin R. Jensen
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#13/Appeal Brief 8/2/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Examiner:	H. Vu	Group Art Unit No.:	2811
Applicant(s):	Pan et al.	Filing date:	May 6, 1998
Serial No.:	09/073,494	For (title):	TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

TRANSMITTAL OF BRIEF ON APPEAL (PATENT APPLICATION — 37 C.F.R. § 192)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the BRIEF ON APPEAL in this application further to the Notice of Appeal filed on June 13, 2000.

2. STATUS OF APPLICATION
   This application is on behalf of
   - ☒ other than a small entity
   - ☐ small entity
     verified statement:
     - ☐ attached
     - ☐ already filed
3. FEE FOR FILING APPEAL BRIEF
   - ☐ small entity status $150
   - ☒ other than a small entity $300
4. EXTENSION OF TIME
   - ☐ A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.
5. FEE PAYMENT
   - ☒ Check No.14329 is enclosed in payment of the fee for filing the Brief on Appeal plus any extension of time for which a petition has been filed.
   - ☐ Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

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Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

~~Adjustment date: 08/22/2000 ETULU1~~
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~~01 FC:119 300.00 OP~~

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Enclosures: As identified above
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Pan et al.

Serial No.: 09/073,494

Filed: May 6, 1998

For: TECHNIQUE FOR ELIMINATION OF PITTING ON SILICON SUBSTRATE DURING GATE STACK ETCH

Examiner: H. Vu

Group Art Unit: 2811

Attorney Docket No.: 2915.1 (96-149.1)

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Devin R. Jensen
Typed/printed name of person whose signature is contained above

BRIEF ON APPEAL

Box AF
Commissioner for Patents
Washington, D.C. 20231
Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is in furtherance of the Notice of Appeal, filed in this case on June 13, 2000, and is submitted in triplicate in the format of 37 C.F.R. § 1.192(c), and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., assignee of the pending application as recorded with the United States Patent and Trademark Office on October 15, 1996, at Reel 8175, Frame 0501.

(2) RELATED APPEALS AND INTERFERENCES

Neither the Applicants, the Applicants' representative, nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 23 through 28 are pending in the application.

Claims 1 through 22 have been canceled.

No claims have been allowed.

Claims 23 through 28 stand rejected.

The rejections of claims 23 through 28 are being appealed.

(4) STATUS OF AMENDMENTS

This Application is a divisional application of Serial No. 08/682,935, filed on July 16, 1996. Claims 1 through 22 were canceled in the Preliminary Amendment dated May 6, 1998, prior to a first office action. Applicants believe that this amendment was entered.

An Amendment in response to the September 23, 1999, Official Action was filed on

December 16, 1999. The response included amendments to claims 23 through 25 and 27 through 28. The December 16, 1999, amendment was submitted to overcome the rejections raised under 35 U.S.C. § 112 (second paragraph), 35 U.S.C. § 102(b) based upon the teachings of United States Patent No. 5,428,244 issued to Segawa et al. and 35 U.S.C. § 102(e) based upon the teachings of United States Patent No. 5,728,625 issued to Tung.

A Final Official Action was mailed on March 14, 2000. A response was submitted on May 16, 2000, in response to the Final Official Action. However, the claims were not amended. The Final Official Action rejected claims 24 and 28 under 35 U.S.C. § 112 (first paragraph) and claims 23 through 28 under 35 U.S.C. § 102 based upon Tung. It is unclear whether or not the rejection under 35 U.S.C. § 102 is based upon § 102(b) or § 102(e) as pointed out in Applicant's response to the Final Official Action. The rejection based upon the Segawa et al. reference was withdrawn.

An Advisory Action was mailed on June 6, 2000, which maintains the rejection of claims 23 through 28 because "Applicant's claims 23-28 does not distinguish over the Tung reference." In response, Applicant's filed a Notice of Appeal on June 13, 2000.

(5) SUMMARY OF THE INVENTION

The present invention relates to gate stacks having minimal or no damage to the gate dielectric layer and/or the silicon substrate. *See, Specification*, p. 2, lines 5-7 and p. 4, lines 16-18. Damage to a gate dielectric layer and/or the silicon substrate results from the formation of silicon clusters in gate stack metallic silicide films. Silicon clusters form within silicon rich metallic silicide films as a result of annealing or exposure to other high temperature steps which

may occur during gate stack formation. *See, Specification*, p. 5, lines 14-17, and 19-21. The etch rate of the silicon clusters is greater than that of the metallic silicide film. Therefore, during the full gate stack etch, silicon clusters within a metallic silicide film are etched faster than the surrounding metallic silicide film. This results in pitting on the gate dielectric layer during the full gate stack etch. *See, Specification*, p. 5, lines 24-28. "By preventing the growth and formation of the silicon clusters in the metallic silicide film, the problem of pitting on the silicon substrate during the gate stack etch can be eliminated." *Specification*, p. 6, lines 3-5, and p. 4, lines 16-18.

One aspect of the present invention eliminates silicon clusters within the metallic silicide film of a gate stack by eliminating the anneal of the metallic silicide film. *See, Specification*, p. 6 lines 8-9. Annealing a metallic silicide film causes the metallic silicide film to form a crystalline structure. *See, Specification*, p. 5, lines 10-11. In addition, "the annealing step causes the silicon within the metallic silicide to form clusters 514 inside the crystalline structured metallic silicide film 502." *Specification*, p. 5, lines 14-15; *see also* p. 6, lines 5-6. Without an anneal of the metallic silicide film, "the metallic silicide film 606 does not form a crystalline structure, nor does it contain silicon clusters." *Specification*, p. 6, line 28 - p. 7, line 1. "The elimination of the formation of the silicon clusters minimizes or eliminates damage to the gate dielectric layer and/or silicon substrate during the gate stack formation." *Specification*, p. 4, lines 16-18.

Silicon clusters may also form in a metallic silicide film during other high temperature processes common to gate stack formation (e.g. over 600°C). The formation of a dielectric cap over the metallic silicide layer is a high temperature process which can cause the formation of silicon clusters. *See, Specification*, p. 5, lines 17-21. Typically, cap formation occurs at over 600°C. By selectively depositing a dielectric cap at temperatures below 600°C the formation of

silicon clusters in the metallic silicide layer can be avoided. *See, Specification*, p. 6, lines 13-18.

Another aspect of the present invention involves the elimination of silicon clusters from a metallic silicide film which has been annealed or exposed to a high temperature process such as cap formation. *See, Specification*, p. 7, lines 5-8. Ion implantation into a silicon cluster containing metallic silicide film disperses the silicon clusters from the metallic silicide film while at the same time amorphizing the metallic silicide film. *See, Specification*, p. 7, lines 6-8. Ion implantation may include the implantation of silicon, tungsten, argon, or the like, or a dopant such as phosphorous, arsenic, boron, or the like. *See, Specification*, p. 7, lines 8-10. Ion implantation energy and dose requirements vary with the the characteristics of the metallic silicide film, the ion used, and the temperature at which the silicon clusters were formed. *See, Specification*, p. 7, lines 12-21.

(6) ISSUES

A. Whether claims 24 and 28 are enabled under 35 U.S.C. § 112, first paragraph, for use of the term "a crystalline metallic silicide film."

B. Whether claims 23-28 are unpatentable as anticipated by United States Patent No. 5,728,625 issued to Tung.

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

Claims 23 through 28 are each separately patentable and claims 23 through 28 do not stand or fall together with respect to the apparent 35 U.S.C. § 102(e) anticipation rejection based

on Tung.

(a) Claim 23 recites a gate stack, including a non-crystalline metallic silicide film.

(b) Claim 24 recites a gate stack, including a crystalline metallic silicide film substantially devoid of silicon clusters.

(c) Claim 25 recites a gate stack having a non-crystalline metallic silicide film disposed over a polysilicon layer.

(d) Claim 26 recites a gate stack structure having a dielectric layer which is substantially devoid of pitting.

(e) Claim 27 stands with claim 26 but does not fall with claim 26 because it recites a gate stack including a non-crystalline metallic silicide film.

(f) With respect to the 35 U.S.C. § 112, first paragraph, rejection, claim 28 stands and falls with claim 24. However, with respect to the 35 U.S.C. § 102(e) anticipation rejection, claim 28 stands with claim 26 but does not fall with claim 26 since it recites a gate stack having a crystalline metallic silicide film substantially devoid of silicon clusters and a dielectric layer substantially devoid of pitting.

(8) ARGUMENT

35 U.S.C. § 112, first paragraph - Claims 24 and 28

Claims 24 and 28 stand rejected under 35 U.S.C. § 112, first paragraph, for allegedly containing subject matter which was not described in the specification is such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Specifically, the Final Office Action has

rejected claims 24 and 28 because the specification allegedly does not disclose that a metallic silicide film is crystalline as claimed.

Contrary to the assertion of the Final Office Action, the term "a crystalline metallic silicide film" as it relates to claims 24 and 28 is described in the disclosure as originally filed. When a metallic silicide film is annealed or exposed to a high temperature cycle, the metallic silicide film forms a crystalline structure. Lines 10 through 11 of page 5 of the Specification explain that it is known in the prior art that a "metallic silicide is annealed to form a crystalline structured metallic silicide film" (emphasis added). Furthermore, in the absence of exposure to a high temperature cycle or an anneal, "the metallic silicide film 606 does not form a crystalline structure." *Specification*, p. 6, line 28 through p. 7, line 1.

In one embodiment of the present invention "the structure 118 is subjected to a heat cycle either to anneal the metallic silicide film 108 prior to depositing the cap 110, to form the cap 110 with a high temperature process (i.e., over 600°C), or both..." *Specification*, p. 9, lines 23-26. As known in the prior art, and as described in the Specification, annealing a metallic silicide film or subjecting a metallic silicide film to a high temperature heat cycle (i.e. over 600°C), forms a crystalline metallic silicide film. *See, supra*. Subjecting the "metallic silicide film 108" to an anneal or a high temperature process would inherently form "a crystalline metallic silicide film" as claimed in claims 24 and 28. Therefore, a gate stack including "a crystalline metallic silicide film" is sufficiently described in the Specification.

One skilled in the art is aware of the processes used to anneal metallic silicide films. Because it is inherent that an annealed metallic silicide film forms a crystalline structure, all that one in the art would have to do to form such a structure is anneal a metallic silicide film or expose

it to a high temperature cycle. Thus, an enabling mode of creating "a crystalline metallic silicide film" would be to anneal the metallic silicide film.

For the foregoing reasons, claims 24 and 28 should be allowed over the Final Office Action 35 U.S.C. § 112, first paragraph, rejection.

35 U.S.C. § 102(e) - the Tung Patent

Claims 23-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tung (United States Patent No. 5,728,625).

Applicants note that the Final Office Action purports to reject claims 23-28 under 35 U.S.C. § 102(e) while providing a recitation of 35 U.S.C. § 102(b) as the basis for the rejection. A rejection of claims 23-28 based upon 35 U.S.C. § 102(b) is improper because Tung was not "patented...more than one year prior to the date of application for patent in the United States." *See*, 35 U.S.C. § 102(b). Therefore, if the actual basis for rejection is 35 U.S.C. § 102(b), Applicants request that the rejection be withdrawn and claims 23-28 allowed.

For the purposes of this Appeal, Applicants assume that the intended basis of rejection of claims 23-28 is 35 U.S.C. § 102(e).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Tung discloses a process for device fabrication in which a layer of cobalt silicide is formed

on a semiconductor substrate as a conductive layer. *Tung* at col. 1, lines 7-9. Tung's invention does not involve the formation of gate stacks. Instead, Tung describes the formation of a gate stack in a process for fabricating n-MOSFET devices. *Tung* at col. 6, lines 55-57. Describing n-MOSFET fabrication, Tung indicates that "the gate electrode 308, is formed <u>using conventional processing techniques</u>." *Tung* at col. 6, lines 64-65 (emphasis added). Tung proceeds to give an example of conventional gate electrode formation techniques:

> For example, a gate insulating film 303, such as a thermally grown SiO_2 film, is formed on the surface of active regions between the field insulating portions 301. Next a polycrystalline silicon film 304 is formed on the surface of the gate insulating film by a CVD (chemical vapor deposition) process, after which a WSi_x layer 305 is sputtered on top of the polycrystalline Si layer 304. An n-type dopant such as As, is then implanted into the WSi_x layer 305 and the upper part of the polycrystalline silicon (Si) layer 304. A hard mask layer 307, such as an SiO_2 layer, is then deposited on the WSi_x layer and the stack of hard mask 307, WSi_x layer 305 and the polycrystalline Si layer 304 is then etched in a desired pattern to form the gate electrode 308 atop the gate insulating film 303 depicted in FIG. 3A.

Tung at col. 6, line 66 through col. 7, line 12. Tung repeats this description, describing another embodiment of Tung's invention. *See, Tung* at col. 8, lines 6-16. Other than these two paragraphs, gate stack formation is not described anywhere else in the Tung reference.

The description of gate stack formation given by Tung describes the sputtering of a WSi_x layer (305) on top of a polycrystalline Si layer. Tung's brief description does not indicate whether the WSi_x layer is annealed or formed at a high temperature such that the WSi_x layer would become crystalline. Tung goes on to describe the implantation of a dopant into the WSi_x layer and the polycrystalline layer. Discussing processes other than gate stack formation, Tung acknowledges that structures must be annealed to electrically activate implanted dopants. *See, Tung* at col. 7, lines 25-28. In any case, if an anneal of the gate stack described in Tung occurred,

it would necessarily follow implantation of the dopant. The activation of the dopant would crystallize the WSi_x layer, resulting in silicon clusters being formed therein. This is consistent with the description of conventional methods of forming gate stacks as described in the Specification. *See, Specification*, p. 3, lines 5-26.

Furthermore, Tung describes the deposition of a hard mask layer (307) such as SiO_2 over the WSi_x layer. Tung is silent as to how, or at what temperature, the hard mask layer is formed. As taught in the context of the present invention, the deposition of SiO_2 cap layers occurs at temperatures over 600°C in conventional gate stack formations. *See, Specification*, p. 3 lines 18-20. A high temperature formation of a hard mask layer anneals the WSi_x layer, which in turn crystallizes the WSi_x layer and forms silicon clusters within the metallic silicide film. *See, Specification*, p. 5, lines 13-15. Tung's process, therefore, would form a silicon cluster containing crystalline metallic silicide film.

Tung also describes the etching of the hard mask layer, the WSi_x layer and the polycrystalline silicon layer to form a desired gate stack formation. Tung does not describe the prevention of pitting on the dielectric layer which occurs during conventional gate stack formations. In fact, Tung does not even acknowledge, or recognize, the problems associated with such pitting or that such pitting is related in any way to the formation of silicon clusters in a metallic silicide film.

Tung's description of gate stack formation is a generalization which is representative of "conventional processing techniques" used to form gate stacks. It is not all-inclusive, and it does not describe the elements of claims 23-28. Specifically, Tung fails to describe the differences between a crystalline and non-crystalline metallic silicide films. Tung also fails to describe the

problems associated with conventional gate stack formation techniques caused by the formation of silicon clusters in metallic silicide films. The lack of description precludes an anticipation rejection under 35 U.S.C. § 102(e).

(a) Claim 23

Claim 23 specifically recites "A gate stack, including a non-crystalline metallic silicide film." The Specification describes a non-crystalline metallic silicide film as a metallic silicide film which is not annealed, has not been exposed to a high temperature process, or which has been amorphized. Tung must describe, either expressly or inherently, a non-crystalline metallic silicide film, or a metallic silicide film which has not been annealed or exposed to a high temperature process in order to anticipate claim 23. Tung fails to do so.

Tung never expressly describes the formation of non-crystalline metallic silicide film. In fact, Tung does not even acknowledge that a metallic silicide film may be crystalline or non-crystalline. Tung expressly describes a conventional gate stack formation which includes the formation of a WSi_x layer, implantation of dopants, and the formation of a hard mask layer. As expressly taught by the present invention, conventional gate stack formation processes produce metallic silicide films which are crystalline. The crystalline nature results from either an anneal of the metallic silicide film or the high temperature formation of a silicon dioxide mask over the metallic silicide film. *See, Specification*, p. 3, lines 12-20. Although Tung does not expressly describe such steps, Tung inherently describes the formation of a crystalline metallic silicide film in a gate stack. Tung describes the doping of the WSi_x layer and the polycrystalline silicon layer during the gate stack formation. Tung also expressly teaches that a structure must be annealed to

activate the dopant. Thus, a crystalline WSi_x layer is inherent in Tung's teaching. Furthermore, it is inherent that the deposition of a hard mask layer is carried out at a high temperature in conventional gate stack formation processes. *See, Specification*, p. 3, lines 18-20. Thus, the WSi_x layer described by Tung would crystallize during the formation of the hard mask layer as described by Tung.

The Final Office Action proposes that "it is inherently [sic] that the tungsten silicide is non-crystalline." *See, Final Office Action* at p. 4, lines 4-5. The basis for this contention rests on the assertion that Tung discloses the deposition of a cobalt silicide layer at a temperature of 450°C, and that the n-type dopant, such as As, implanted in the tungsten silicide amorphizes the silicide film. *See, Final Office Action*, pp. 3-4, ¶ 3. Neither of these assertions provides a basis for finding that Tung inherently describes a gate stack having a non-crystalline metallic silicide film.

Tung describes the formation of an <u>annealed</u> cobalt silicide layer occurring between a temperature of about 450°C and about 800°C. *See, Tung* at col. 6, lines 11-18. The temperature of formation is irrelevant because <u>the cobalt silicide layer is annealed, which inherently indicates that it has a crystalline structure</u>. *See, Specification*, p. 5, lines 10-11. Furthermore, Tung's description of the cobalt silicide film is not a description of the formation of a metallic silicide film layer in a gate stack formation. Rather, the cobalt silicide film disclosed by Tung pertains to Tung's invention, a conductive silicide layer overlying a semiconductor substrate. The annealed crystalline cobalt silicide layer of Tung does not expressly or inherently describe a non-crystalline metallic silicide layer in a gate stack as claimed in claim 23.

Tung's description of the implantation of n-type dopants, such as As, into the WSi_x layer

during gate stack formation also fails to inherently describe a non-crystalline WSi_x layer. As explained above, the implantation of dopant into the WSi_x layer occurs prior to the formation of the hard mask layer of the gate stack. The formation of a hard mask layer inherently involves a high temperature cycle which would anneal the WSi_x layer, thereby forming a crystalline structure. *See, Specification*, p. 3, lines 18-22, and p. 5, lines 17-23. Furthermore, Tung expressly indicates that a device implanted with dopants must be annealed to electrically activate the dopants. This inherently indicates that the WSi_x layer of Tung would be annealed following the implantation of the dopant, thereby forming a crystalline WSi_x layer. The contention that the presence of dopant impurities prevents a WSi_x layer from crystallizing is not described anywhere in the reference and therefore does not inherently describe a non-crystalline metallic silicide layer in a gate stack.

Tung's failure to describe, either expressly or inherently, a non-crystalline metallic silicide film in a gate stack precludes the anticipation rejection under 35 U.S.C. § 102(e). Applicants respectfully request the allowance of claim 23.

(b) Claim 24

Claim 24 recites "A gate stack, including a crystalline metallic silicide film wherein said metallic silicide film is substantially devoid of silicon clusters." As taught by the present invention, when a metallic silicide film is annealed, it forms a crystalline structure. *See, Specification*, p. 5, lines 10-11. Furthermore, annealing a metallic silicide film, or exposing a metallic silicide film to a high temperature cycle, causes the formation of silicon clusters within the metallic silicide film.

Tung does not describe, either expressly or inherently, the crystalline nature of an annealed

metallic silicide film. Tung also fails to describe the formation of silicon clusters in metallic silicide films or the problems associated therewith. The failure of Tung to expressly or inherently describe these aspects of claim 24 precludes the anticipation rejection of claim 24. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Furthermore, the Final Office Action argues that Tung discloses "a non-crystalline silicide film disposed over the polycrystalline layer" (emphasis added). This argument in and of itself precludes the rejection of claim 24, because it implies that Tung does not teach a crystalline metallic silicide film. However, Applicants assert that Tung necessarily describes a crystalline metallic silicide film having silicon clusters formed therein.

As discussed with respect to claim 23 above, Tung's description of gate stack formation inherently describes a crystalline metallic silicide film. The formation of a crystalline metallic silicide film causes silicon clusters to form within the metallic silicide film. *See, Specification*, p. 13-15. Thus, Tung's description of a gate stack inherently includes the formation of silicon clusters within the WSi_x layer. Claim 24 however, recites a crystalline metallic silicide film "substantially devoid of silicon clusters." The Specification supports this claim, teaching that silicon clusters within a crystalline metallic silicide film may be dispersed by the implantation of ions into the metallic silicide film following an anneal or high temperature exposure. *See, Specification*, p. 7, lines 5-21. Tung does not describe such a process, or a crystalline metallic silicide film substantially devoid of silicon clusters.

The Final Office Action implies that the implantation of As in the WSi_x layer, as described in Tung, would amorphize the WSi_x layer and disperse any existing silicon clusters. However, as mentioned with respect to claim 23 above, the implantation of As occurs prior to the final

crystallization of the WSi_x layer. Tung implies that the WSi_x layer is annealed following the dopant implantation to electrically activate the impurities. Tung also describes the deposition of the hard mask layer over the WSi_x layer following doping which inherently forms silicon clusters in the WSi_x layer. *See, Specification*, p. 5, lines 17-21. Thus, Tung fails to either expressly or inherently describe a gate stack as claimed in claim 24.

(c) Claim 25

Claim 25 recites a gate stack comprising, among other elements, "a non-crystalline metallic silicide film." Tung neither expressly nor inherently describes a gate stack having such a limitation.

As pointed out with reference to claim 23 above, the gate stack formation process of Tung inherently describes the formation of a crystalline metallic silicide film. Tung does not describe the formation of a gate stack having a non-crystalline metallic silicide film. In fact, Tung does not even draw a distinction between a crystalline and a non-crystalline metallic silicide film in a gate stack. Tung's failure to expressly or inherently describe gate stack having a non-crystalline metallic silicide film in as complete detail as is recited in claim 25 precludes the anticipation rejection. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(d) Claim 26

Claim 26 recites "A gate stack structure comprising a gate stack on a dielectric layered semiconductor substrate wherein said dielectric layer is substantially devoid of pitting." As taught in the present invention, the formation of silicon clusters in a metallic silicide film results in an

increased gate stack etch rate, which, in turn, causes pitting within the dielectric layer. The absence of silicon clusters in a metallic silicide film, however, prevents pitting in the dielectric layer.

Tung fails to anticipate claim 26 because Tung does not describe, either expressly or inherently, a gate stack having a dielectric layer substantially devoid of pitting. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The Final Office Action bases the rejection of claim 26 on the contention that "because the silicide film is substantially devoid of silicon clusters, it is inherently [sic] that the dielectric layer is substantially devoid of pitting." *See, Final Office Action* at p. 4, lines 6-9. This rejection thus relies upon the teachings of the present invention and not those of Tung. Tung does not describe a silicide film substantially devoid of silicon clusters, and therefore, it is not inherent that the dielectric layer of Tung is devoid of pitting. Furthermore, Tung fails to even recognize, much less describe, why pitting may or may not occur. Thus, Tung cannot describe an inherent solution to a problem which Tung does not acknowledge.

(e) Claim 27

Claim 27 stands with claim 26, but does not fall with claim 26 because in addition to claiming a dielectric layer substantially devoid of pitting, claim 27 also recites that the gate stack includes "a non-crystalline metallic silicide film."

As set forth in detail previously with respect to claims 23 and 25, Tung does not describe the claimed non-crystalline metallic silicide film. Tung never acknowledges that a metallic silicide film may be crystalline or non-crystalline. Instead, Tung generally describes a gate stack

formation process which inherently forms a crystalline metallic silicide film. The process of annealing the WSi_x layer of Tung to dope the polycrystalline silicon layer and the inherent high temperature step required to form the hard mask layer, result in a crystalline metallic silicide film. Thus Tung fails to describe a non-crystalline metallic silicide film.

Furthermore, as recited with respect to claim 26, Tung does not describe a dielectric layer substantially devoid of pitting. Tung does not even acknowledge that pitting occurs on a dielectric layer in a gate stack formation. Tung does indicate that the gate electrode described by Tung is made using conventional processing techniques. As pointed out by the present invention, it is such conventional techniques which result in the problem of pitting on the dielectric layer. *See, Specification*, p. 3, lines 5-26.

Tung's failure to describe both a non-crystalline metallic silicide film and a dielectric layer substantially devoid of pitting precludes the anticipation rejection. *See*, *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

(f) Claim 28

Claim 28 stands with claim 26, but does not fall with claim 26 because in addition to claiming a dielectric layer substantially devoid of pitting, claim 28 recites "a crystalline metallic silicide film substantially devoid of silicon clusters" which is not described by Tung.

As with claims 27 and 26, Tung does not describe, either expressly or inherently, a dielectric layer substantially devoid of pitting. Therefore, Tung does not anticipate claim 28. *See*, *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Furthermore, Tung fails to describe a crystalline metallic silicide layer substantially devoid

of silicon crystals. Tung's brief and conventional description of a gate stack formation inherently describes a gate stack having a silicon clustered, crystalline metallic silicide film. *See, Section 8(b)* above. Tung does not describe, nor even mention, a metallic silicide film devoid of silicon clusters, and therefore, can not anticipate claim 28. *See*, *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

APPENDIX

23. A gate stack, including a non-crystalline metallic silicide film.

24. A gate stack, including a crystalline metallic silicide film wherein said metallic silicide film is substantially devoid of silicon clusters.

25. A gate stack on a dielectric layered semiconductor substrate, comprising:
a polysilicon layer disposed over said dielectric layered semiconductor substrate;
a non-crystalline metallic silicide film disposed over said polysilicon layer; and
a dielectric cap on said non-crystalline metallic silicide film.

26. A gate stack structure comprising a gate stack on a dielectric layered semiconductor substrate wherein said dielectric layer is substantially devoid of pitting.

27. The gate stack structure of claim 26 wherein said a gate stack includes a non-crystalline metallic silicide film.

28. The gate stack structure of claim 26 wherein said a gate stack includes a crystalline metallic silicide film substantially devoid of silicon clusters.

Respectfully submitted,

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